USB 3.1 Specification
1.0 Release Seminar
Taipei, Taiwan
December 10, 2013
Seminar Agenda

8:00 Registration check-in
9:00 Introduction to 10Gbps SuperSpeed USB
9:20 Architectural Overview
10:00 Break
10:30 Cables and Connectors
11:00 Physical Layer
12:00 Lunch
1:00 Link Layer
2:00 Protocol Layer
2:30 Break
3:00 Hub
4:00 Compliance
4:15 Q&A Session
4:30 Close
Seminar Agenda – Bonus Session

Wednesday, December 11, 2013

9:00 - Noon  USB 3.1 Electrical Design
Howard Heck & Jennifer Tsai

• Introduction
  • Interoperability goals, target design envelope
• System Analysis
  • Reference channels, usage recommendations
• Channel Design
  • Packages, PCBs, connectors
• Equalizer Design
  • Goals, TxEQ, RxEQ
• Design for EMC & RFI
• Repeaters
Introduction

USB 3.1 SuperSpeed

- Motivation
- Use Cases for USB 3.1 SuperSpeed
- Proposed Approach
- Spec Development Process and Timeline

Bob Dunstan
Brad Saunders
Intel
Motivation

USB 3.0 SuperSpeed @ 5Gbps is enabling new usages
• Compelling video display – 1080p/60fps (uncompressed)
• High-performance storage – 450MB/sec SSDs
• USB docking – multi-function hubs

Usage assessment indicates increase in BW needed to dramatically improve USB experience
• Display + storage + other features can saturate 5Gbps
• SSD and hybrid HDDs on track to break 500MB/sec within three years

Technical analyses indicate that a doubling of data rate “within” the existing ecosystem is feasible
Use Cases for USB 3.1

Support attach of much higher performance peripherals
- A/V Display beyond 1080p (uncompressed) and multi-displays
- SSD, RAID HDD, or Hybrid HDD

Blazing fast data sync

Enable multi-function, single port connections
- SuperSpeed Hubs with fatter system pipe supporting multiple SuperSpeed downstream devices
- Display Dock enabling mix of SuperSpeed-based A/V, webcam, storage, etc. over a single connection
USB 3.1 Specification

• Started with the USB 3.0 specification
  • Integrated the outstanding ECNs then ...

• Added 10Gbps SuperSpeed
  • Connector
  • PHY and Link
  • Protocol, Framework and Hub

• Resulting spec supersedes previous USB 3.0 specification
Approach

Double USB SuperSpeed bandwidth by adding 10Gbps data rate
  • Enable across existing USB connectors with full backward compatibility
    – Normalize requirements based on 1m cable usage
  • Auto negotiation to the highest mutually supported data rate
  • Extend hub definition to address rate matching and optimize upstream channel utilization
  • Address RFI compatibility with wireless applications
  • Power efficiency should be equal or better than 5Gbps SuperSpeed

No changes required in software stack and xHC comprehends BW scaling
Updated compliance plans/specs to be developed
Investigate if additional design guidance/specs are needed for successful platform and device implementation
Specification Development Process

Implemented as a update to the USB 3.0 spec

- New speed mode is variant of SuperSpeed

Spec development was done by a WG under the USB 3.0 Promoter Group structure

- Same as USB 3.0 Specification
- Extended 0.7 and 0.9 industry reviews to all interested USB 3.0 Contributors
- Feedback incorporated into the subsequent revisions
Specification Timeline

**Specification Development**

- **Initial Product Development**
- **Compatibility Development**
- **Initial Silicon Development**
- **Industry Review #1**
- **Industry Review #2**
- **Compliance Development**
- **DevCons**

**Timeline**

- **Jan**
- **Feb**
- **May**
- **Q3**
- **Q4**

**Years**

- **2013**
- **2014**

**Drafts**

- **0.7 Draft**
- **0.9 Draft**
- **1.0 Final**

**Related Documents**

- Universal Serial Bus 3.0 Specification (Including 10Gbps SuperSpeed Extensions)
- Universal Serial Bus 3.1 Specification (Including errata and ECHs through May 10, 2013)
- Universal Serial Bus 3.1 Specification
Architectural Overview

• Team Introduction
• Terminology update
• System Goals
• Chapter Highlights
• Related Specs
• Need your input

Bob Dunstan
Intel
Team

Overall Dublin Spec
- Bob Dunstan – Intel
- Tony Priborsky – Seagate

CabCon
- Yun Ling – Intel
- Alvin Cox – Seagate

Physical Layer
- Howard Heck - Intel
- John Stonick – Synopsis

Link Layer
- Huimin Chen – Intel
- Peter Teng - Renesas

Protocol
- Bob Dunstan – Intel
- Sue Vining - TI

Hub
- Rahman Ismail – Intel
- John Garney - MCCI

xHCI
- Steve McGowan – Intel

Pipe
- Dan Froelich – Intel

Historian
- John Howard -Intel
Terminology Changes

• *SuperSpeed* was used to describe the 5Gb signaling speed and the architectural extensions
• USB 3.1 SuperSpeed doubles speed and introduces architectural extensions
• New terms were needed to distinguish between
  • Basic SuperSpeed items that are not speed dependent
  • Items that are specific to speed, i.e., 5Gbps, 10Gbps and future “speeds and feeds”
  • 10Gbps and greater architectural extensions
## New Terminology

<table>
<thead>
<tr>
<th>Gen 1</th>
<th>Operating at 5Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen 2</td>
<td>Operating at 10Gbps</td>
</tr>
<tr>
<td>Gen X</td>
<td>Operating at either 5Gbps or 10Gbps</td>
</tr>
<tr>
<td>SuperSpeed Host/Device/Hub</td>
<td>The portion of a USB 3.1 Device/Hub/Host that supports Gen 1 speed</td>
</tr>
<tr>
<td>SuperSpeed</td>
<td>Could be bus, system, etc. that supports Gen 1 speed</td>
</tr>
<tr>
<td>SuperSpeedPlus</td>
<td>Could be bus, system, etc. that supports above Gen 1 speeds</td>
</tr>
<tr>
<td>SuperSpeedPlus Host/Device/Hub</td>
<td>The portion of a USB 3.1 Device/Hub/Host that supports above Gen 1 speeds</td>
</tr>
<tr>
<td>Enhanced SuperSpeed speeds</td>
<td>Gen 1 and above speeds</td>
</tr>
<tr>
<td>Enhanced SuperSpeed port</td>
<td>A port that supports Gen1 and above speeds</td>
</tr>
</tbody>
</table>

Common abbreviations:  SS = SuperSpeed  SSP = SuperSpeedPlus
System Goals

• Double bandwidth
  • On the link
  • Through the fabric

• Preserve/improve power efficiency

• No OS driver changes required
  • Just works by default
  • For some cases, driver enhancements will be needed to allow devices to take advantage of new capabilities (e.g. 750 MB/s ISO)
Mechanical

• New channel budget definition
• Support 1M cable
• Backwards compatible connectors
• Insertion Detect and PD compatibility
Physical Layer

• More than double bandwidth
  • 10 Gbps signaling rate
  • 128b/132b line code
    – 20% additional BW over 8b10b

• New channel definition
  • Move to equal channel allocation for both host and device

• LFPS extended (LBPM)

• Requirements for Retiming Repeaters will be added in Appendix E
Link Layer

- Updated LTSSM to handle multiple speeds
- Link Speed negotiation / training
- Equivalent or better error rates
  - Frame markers - bit error tolerant
  - DPH – appends redundant length info
- Preserved framing to maximize similarity with SuperSpeed
- Added a second Link credit class
LTSSM State Machine

Diagram showing state transitions and conditions, such as power on reset, warm reset, removal, Rx detect, and other events leading to states like SS.Inactive, SS.Disabled, and states with timeouts such as LFPS, Polling, and Recovery.
Protocol Layer

New

- **Support for multiple INs**
  - Used by hubs to maximize throughput in mixed speed topology
  - Ordering rules for multiple in-flight INs
- **Precision Time Management (USB 3.0 ECN)**
  - ITPs still used but are more precise when PTM is present

Changes

- **Expanded header definition**
  - Added field to identify transaction type
  - Extended the use of the Route String field to include a weight for device to host Data Packets
- **Increased Isochronous maximum bandwidth**

Deprecated

- **Num HP, Link Speed fields in config LMPs**
- **Bus Interval Adjustment**
  - Device Notification / Message
Hub

• Add store and forward model for DPs
• Maximized utilization of upstream link
  – Multiple in-flight INs
  – Reordering of DPs
• Fair share of BW regardless of place in topology
• Two link credit classes ensure link/connection management TPs can flow
• Buffering increased
• UFP and DFP state machines updated
xHC - Requirements

• Don’t break legacy software
  – Hardware-based Enhanced SuperSpeed speed notification mechanism

• Enable xHC to schedule SuperSpeedPlus devices to maximize bus utilization
  – Support multiple INs for devices operating at Gen 2 speed
  – Take advantage of additional bandwidth

• Enable easy future extension
xHC - Speed Reporting

Link Speed Device Notification TP

• Received from device after it enters the Address State
• xHC matches the Link Speed Notification to closest Speed ID
  – Updates Slot Context
• xHC uses the new Speed to adjust its scheduling algorithm to the device
• Software can optionally enable Link Speed Device Notification Events
PIPE Spec with USB 3.1 Updates

USB 3.1 updates use same signals as PCI Express* 3.0 PIPE
128/130 support with two additional header bits
  - TxDataValid, RxDataValid
  - TxStartBlock, RxStartBlock
  - TxSyncHeader[3:0], RxSyncHeader[3:0]
  - Header error detection/reporting handled by controller
  - Polarity detection handled by controller

PIPE 4.2 with USB 3.1 updates based on .9 rev USB 3.1 specification available for review

PIPE 4.3 with USB 3.1 comments and updates for 1.0 planned release Q3/Q4 2013
Compliance

Enhanced SuperSpeed Hosts/Devices will be tested for:

- Compliance at the USB 2.0 speeds supported
- Compliance to SuperSpeed USB requirements
- Compliance to new SuperSpeedPlus USB requirements

SuperSpeedPlus USB Compliance Requirements

- Interoperability test will be updated to include support for SuperSpeedPlus hosts/devices
- Use the same backwards compatibility tests
- Updated framework tests
- New link layer tests
- New electrical tests for the physical layer
- Additional cable tests for channel and power
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Cables and Connectors

- Requirements and Scope
- Changes and Additions
- Performance Improvements
- Compliance methodology
- Summary

Yun Ling / Intel
Alvin Cox / Seagate
Requirements and Scope

1. Backward compatible with existing USB 3.0 connectors
   • No change in mating interfaces
   • Support all existing USB 3.0 connectors except Power-B

2. Improving connector/cable electrical performance and compliance methodology to support 10 Gbps channel

3. No new connector form factor
Changes and Additions
Spec Clean-ups

Spec clean-up done where necessary
Standard-A with Insertion Detect

Added Std-A connector drawings illustrating Insertion Detect

Insertion Detect is specified in the USB PD spec to provide a means for Std-A cold socket
Footprints

Added additional reference footprints

- The Reverse and mid-mount (or sink-mount) Std-A connector footprints due to their increasing need
  - Driven by low z-height requirement

Standard-A Reverse Mount

Standard-A Middle Mount
Reference Footprint Pad Stack-ups

To ensure good high speed performance, reference pad stack-ups (hole, pad, anti-pad size / ground plane cutouts) are shown to provide insight as to how to properly design PCBs for optimum electrical characteristics.

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Finished hole radius</td>
<td>0.35</td>
</tr>
<tr>
<td>b</td>
<td>Annular ring radius</td>
<td>0.50</td>
</tr>
<tr>
<td>R</td>
<td>Antipad radius to center</td>
<td>0.75</td>
</tr>
<tr>
<td>P</td>
<td>Antipad center to center distance</td>
<td>2.00 (Std-A) 1.75 (Std-B)</td>
</tr>
</tbody>
</table>

Unit: mm
EMI/RFI Contacts

Added (additional) EMI/RFI grounding fingers in the Stand-A connector and defined their contact zones (required)

- To mitigate the RFI issues reported for USB 3.0 Gen1

*TOP VIEW (SIDE NEAREST SUPERSPEED CONTACTS)*
Cable Shielding Effectiveness

Added a new section requiring cable shielding effectiveness to manage cable radiation

- Technical details about the testing and pass/fail criterion are still under development

5.6.1.3.2.7 Cable Shielding Effectiveness

The cable assembly shielding effectiveness (SE) test measures the radio frequency interference (RFI) level from the cable assembly. To perform the measurement, the cable assembly shall be installed in the cable SE test fixture as shown in Figure 5-29. The coupling factors from the cable to the fixture are characterized. The Cable SE test fixtures and specification values are under development and are to be included in future updates to this specification.
Electrical Performance Improvement

• The mated cable assembly insertion loss is budgeted to be $\leq 6$ dB @ 5 GHz
  • Targeted for 1 meter, *not* 3 meters
  • Longer than 1 meter may require an active cable

• Both raw cable and connector performance needs improvement to achieve this

• EMI/RFI performance improvement required
Performance Improvements
Raw Cables

- Raw cable with better loss characteristics needed
- Coaxial cable option included, besides SDP (shielded diff pair)
- With improved performance, 34 AWG can reach ~1 m

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>SDP Differential Insertion Loss (dB/m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.625</td>
<td>-2.7/1.3/1.0/-0.9</td>
</tr>
<tr>
<td>1.25</td>
<td>-3.3/-1.9/-1.5/-1.3</td>
</tr>
<tr>
<td>2.50</td>
<td>-4.4/-3.0/-2.5/-1.9</td>
</tr>
<tr>
<td>5.00</td>
<td>-6.7/-4.6/-3.6/-3.1</td>
</tr>
<tr>
<td>7.50</td>
<td>-9.0/-5.9/-4.7/-4.2</td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>SDP Differential Insertion Loss Examples for SS+</th>
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<td>Frequency (GHz)</td>
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<td>5.00</td>
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</tr>
<tr>
<td>5.00</td>
</tr>
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<td>7.50</td>
</tr>
</tbody>
</table>

Differential Insertion Loss Examples for SS+ with Coaxial Construction
Connectors
Efforts have been made to each section of the connector subsystems to minimize reflection and crosstalk

- Footprint and pad-stackup
- Contact Optimization
- Connector subsystem optimization
- Wire Termination
A Closer Look at the Connectors

- Receptacle Contact
- Mating Interface
- Wire Termination
- Plug Contact

- PCB Launch

Ground voiding

(a) Poorly managed wire termination

(b) Well managed wire termination
Connector Performance Improvements

Significant improvement achieved in impedance match and crosstalk reduction!
- Less ripples in insertion loss
- Watch for xtalk between D+/D- and SSP for Std A connector

Between SS+

Between D+/D- and SS+
EMI/RFI Improvement

Improvement mainly comes from the increase number of EMI/RFI grounding fingers – from three to seven

Probe placed near USB3 Connector

Power [dBm/100kHz]

Frequency [GHz]

-120  -115  -110  -105  -100  -95  -90  -85  -80

2.4  2.42  2.44  2.46  2.48  2.5

Original Connector

With ground improvement

No USB3 Device

Ambient Noise
Compliance Methodology Improvement

Conventional ways to specify cable/connector electrical requirements have flaws

- S-parameter envelopes or time-domain peak values are not always good measurement of performance

Will this spec violation really cause a failure?

Is peak-to-peak crosstalk the only thing we need to worry about?
New Compliance Methodology

A new compliance methodology is used for the cable assembly

- Uses reference PHYs for the host and device
- Metrics include:
  - Insertion loss fit at Nyquist frequency (ILfitatNq)
  - Integrated multi-reflection (IMR)
  - Integrated crosstalk (IXT)

Ref Host

Cable Assembly

Ref Device
About the Metrics

It is a figure of merits of channel quality, representing channel signal integrity impairments: attenuation, reflection and crosstalk

\[
IMR = \sqrt{\int [ILD(f)]^2 |V_m(f)|^2 df} / f_{3dB} \times 1000 \text{ (in mV).}
\]
Pass/fail Criteria
Based on channel eye height (eH) and/or eye width (eW) instead of component S-parameters profiles

Prediction formulae:
\[ eH = f_H(ILfitatNq, IMR, IXT) \]
\[ eW = f_W(ILfitatNq, IMR, IXT) \]

Pass/fail Criteria:
\[ eH = f_H(ILfitatNq, IMR, IXT) > 0 \]
\[ eW = f_W(ILfitatNq, IMR, IXT) > 0 \]
\[ ILfitatNq \geq -22 \text{ dB} \]
\[ IMR \leq 60 \text{ mV} \]
\[ IXT \leq 25 \text{ mV} \]
Cable/Connector Summary

• No new mechanical interface defined
• Changes are mainly driven by the data rate doubling!
  • Improvement in EMI/RFI performance was also needed
• Most spec development efforts focused on cable and connector electrical performance improvements
• Cable assemblies will be tested with a new compliance methodology to make testing more meaningful
• Mechanical team is currently focusing on signal integrity and EMI/RFI compliance documents development
Physical Layer

- Gen 2 Reference Transmitter
- Gen 2 Reference Receiver
- Gen 2 Signal Encoding
- New LFPS Signaling

Howard Heck
Intel

John Stonick
Synopsys
Reference Transmit Equalization

• Tx equalization is not normative for Gen 2 operation
  • No one setting is best for all designs
  • Want to avoid Tx adaptation and back channel
  • Meeting far end compliance is important
    – Allow freedom for system developers to optimize transmitter settings

• Two recommended settings provided
  • System simulations showed good performance across a variety of lines
  • These are provided as guidance – not a mandate
Reference Transmit Equalization

Host/device loss = differential insertion loss from silicon die pad to connector:
- parasitic I/O capacitance
- chip package (routing, vias, I/O pins)
- PCB (routing and vias)

Recommended TxEQ Settings

<table>
<thead>
<tr>
<th>Host/Device Loss</th>
<th>&lt;3.5dB</th>
<th>≥3.5dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{-1}</td>
<td>0.000</td>
<td>-0.125</td>
</tr>
<tr>
<td>C_{1}</td>
<td>-0.100</td>
<td>-0.125</td>
</tr>
<tr>
<td>Va/Vd</td>
<td>1.00</td>
<td>0.80</td>
</tr>
<tr>
<td>Vb/Vd</td>
<td>0.75</td>
<td>0.55</td>
</tr>
<tr>
<td>Vc/Vd</td>
<td>0.75</td>
<td>0.75</td>
</tr>
</tbody>
</table>
Reference Receiver Equalization

- Reference receiver equalizer used to setup for transmitter compliance testing
  - Eye quality measured at output of adapted (optimized) Rx equalizer
  - Test equipment will have this equalizer for processing the data
- Target channel loss for system is 20db die pad to die pad
  - Combination of Tx settings and Rx equalization ranges sufficient for target loss
  - Repeaters will be needed for worse channels
Reference Receiver Equalizer

Uses:
- Transmitter compliance testing
- Behavioral reference for receiver design

\[ y_k = x_k - d_1 \text{sgn}(y_{k-1}) \]
\[ 0 \leq d_1 \text{sgn}(y_{k-1}) \leq 50mV \]
Transmitter Compliance Eye Mask

- Eye height = worst case measured (center ± 0.05UI)
- Eye width extrapolated to 1e-12 BER
- Measured after reference receiver equalizer

Measure over $10^6$UI
## Link Budgets

### Jitter
- Channel jitter includes crosstalk & ISI after equalization.
- Budget is basis for compliance:
  - Tx compliance eye
  - High freq input jitter for Rx compliance

<table>
<thead>
<tr>
<th>Term</th>
<th>DJ (ps)</th>
<th>RJ (ps)</th>
<th>TJ (ps)</th>
<th>( \sigma_{RJ} ) (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx</td>
<td>17.0</td>
<td>18.4</td>
<td>35.4</td>
<td>1.307</td>
</tr>
<tr>
<td>Channel</td>
<td>36.0</td>
<td></td>
<td>36.0</td>
<td></td>
</tr>
<tr>
<td>Rx</td>
<td>21.0</td>
<td>18.4</td>
<td>39.4</td>
<td>1.307</td>
</tr>
<tr>
<td>Total</td>
<td>74.0</td>
<td>26.0</td>
<td>100.0</td>
<td>1.85</td>
</tr>
</tbody>
</table>

### Loss
- Cable assembly includes the mated pairs at both ends.
- Host/device includes I/O parasitics, package & PCB.
Gen 2 “Golden PLL” and JTF for Tx Jitter

JTF corner at 7.5MHz
SSC df/dt Limits

• Previous standard did not have a df/dt profile.
  ▪ Phase slew limit did not limit max df/dt

• This type of limit has appeared in other standards.

• New limit is 1250ppm/us measured over 0.5us.

• Measured profile is smoothed with a filter, the precise filter has a 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be greater or equal to a second order low-pass of 20 dB per decade.

• Triangular profile is approximately 5000/16.67us = 300ppm/μs.
Receiver

• Receiver stress tested through JTOL.
  • Reference transmitter tuned to provide minimal compliant eye at output of reference receiver equalizer.
  • Reference equalizer (scope) replaced with DUT board.
  • Link is brought up and receiver is allowed to adapt.
  • JTOL is measured.

• Receiver will have to be at least as capable as reference receiver.
## Receiver Jitter Tolerance

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Gen 1</th>
<th>Gen 2</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>f1</td>
<td>Tolerance corner</td>
<td>4.9</td>
<td>7.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>J_{Rj}</td>
<td>Random Jitter</td>
<td>0.0121</td>
<td>0.01308</td>
<td>UI rms</td>
<td>1</td>
</tr>
<tr>
<td>J_{Rj,p-p}</td>
<td>Random Jitter peak- peak at 10^{-12}</td>
<td>0.17</td>
<td>.184</td>
<td>UI p-p</td>
<td>1,4</td>
</tr>
<tr>
<td>J_{Pj,500kHz}</td>
<td>Sinusoidal Jitter</td>
<td>2</td>
<td>2.56</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{Pj,1Mhz}</td>
<td>Sinusoidal Jitter</td>
<td>1</td>
<td>1.28</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{Pj,2MHz}</td>
<td>Sinusoidal Jitter</td>
<td>0.5</td>
<td>0.64</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{Pj,4MHz}</td>
<td>Sinusoidal Jitter</td>
<td>N/A</td>
<td>0.32</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{Pj,f1}</td>
<td>Sinusoidal Jitter</td>
<td>0.2</td>
<td>0.17</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{Pj,50MHz}</td>
<td>Sinusoidal Jitter</td>
<td>0.2</td>
<td>0.17</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>J_{Pj,100MHz}</td>
<td>Sinusoidal Jitter</td>
<td>N/A</td>
<td>0.17</td>
<td>UI p-p</td>
<td>1,2,3</td>
</tr>
<tr>
<td>V_{full_swing}</td>
<td>Transition bit differential voltage swing</td>
<td>0.75</td>
<td>TBD</td>
<td>V p-p</td>
<td>1</td>
</tr>
<tr>
<td>V_{EQ_level}</td>
<td>Non transition bit voltage (equalization)</td>
<td>-3</td>
<td>Pre=2.7, Post=-3.3</td>
<td>dB</td>
<td>1</td>
</tr>
</tbody>
</table>

**Notes:**
1. All parameters measured at TP1. The test point is shown in Figure 6-18.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate J\_p\_j at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in Figure 6-19.
Ordered Sets

- **TS1, TS2, TSEQ, SKP, SDS, SYNC**
- New SYNC ordered set has two purposes
  - SYNC OS can be used to achieve frame alignment
  - Tx Scrambler reset after last Symbol of SYNC OS is sent
  - Rx Scrambler reset after last Symbol of SYNC OS is received
- Ordered sets defined before scrambler
  - Each ordered set is defined by 128 bits
  - Period of scrambled ordered set (receiver input) depends upon reset period of scrambler
Gen 2 TS Ordered Sets

• TS1 and TS2
  ▪ Symbol 0 is not scrambled
  ▪ Symbols 1-13 are always scrambled
  ▪ Last two Symbols of ordered set will be used for DC balance if necessary otherwise they are scrambled
  ▪ SYNC inserted every 32 blocks. Patterns repeat every $32 \times 132 = 4224UI$
  ▪ SKPs can interrupt pattern

• TSEQ
  ▪ Symbols 0-13 are scrambled
  ▪ Last two Symbols of ordered set will be used for DC balance if necessary otherwise they are scrambled
  ▪ Pattern is periodic in $16384 \times 132UI = 2162688UI$
  ▪ No SKP OSs inserted into pattern
Gen 2 SKP Ordered Set

• Not scrambled
• Scrambler does not advance while sending or receiving a SKP ordered set
• Transmitted SKP OS is 16 Symbols
• Received SKP OS can be 0 to 36 SKP Symbols (add/remove 2 SKP Symbols at a time)
• Last 4 Symbols describe the present state of the LFSR23 scrambler
Gen 2 Compliance Patterns (at 10Gb/s)

- **CP 9**: Gen 2 compliance pattern
  - SYNC followed by 16368 (16384-16) symbols of scrambled 00h
  - Used for compliance testing

- **CP 10**: AAh
  - Unscrambled Nyquist as debug aid
  - Measure RJ

- **CP 11**: CCh
  - Unscrambled Nyquist/2 as debug aid
  - Measure RJ without DCD

- **CP 12**: LFSR15, G(X) = TBD
  - Unscrambled LFSR15 for debug and fault isolation
  - Easy to add BERT in PMA to check this pattern
Polling.LFPS

- SCD1.LFPS (4’b0010), and SCD2.LFPS (4’b1101) similar to TS1/TS2 handshake for declaring SSP identity.
- Gen 2 port shall transmit SCD1.LFPS. If SCD1.LFPS cannot be found in at least 16 consecutive Polling.LFPS received, it shall transmit Polling.LFPS of Gen 1 characteristics instead of SCD1.LFPS.
- Return to SS mode when long duration of electrical idle are observed (assuming connected SS device has entered Polling.RxEQ in transmitting TSEQ ordered set). SSP device is not required to enable SS receiver for TSEQ training until some duration (~60us) of electrical idle is observed. 60us out of 4ms (needed in 64K TSEQ ordered set) should not be critical for SS training.
LFPS Based PWM Signaling (LBPS)

<table>
<thead>
<tr>
<th></th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>tLFPS-0</td>
<td>1/4 tPWM</td>
<td>1/3 tPWM</td>
</tr>
<tr>
<td>tLFPS-1</td>
<td>2/3 tPWM</td>
<td>3/4 tPWM</td>
</tr>
</tbody>
</table>

tPWM will be between 2μs and 2.4μs
longest tLFPS-0 = 0.8μs, shortest tLFPS-1 = 1.3μs
LFPS Based PWM Signaling (LBPS)

<table>
<thead>
<tr>
<th>Unit</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>TYP</td>
</tr>
<tr>
<td>tPWM</td>
<td>2</td>
<td>2.2</td>
</tr>
<tr>
<td>tLFPS-0</td>
<td>0.5</td>
<td>0.80</td>
</tr>
<tr>
<td>tLFPS-1</td>
<td>1.33</td>
<td>1.80</td>
</tr>
</tbody>
</table>
• Byte-based messages; lsb first.
  ▪ Start with 1 tPWM of LFPS, followed by 1 tPWM of EI
  ▪ End with 1 tPWM of LPFS

• LPBM messages are defined in the Polling.PortMatch substate (Chapter 7.5.4.5)
Repeaters

- The compliance testing environment will be built around the loss budget on the right.
- May need a repeater if your host or device loss exceeds 7dB at 5GHz.
Repeater Requirements & Schedule

Expected implementation

• Same transmitter & receiver specs as for hosts and devices.
• Elastic buffer and SKP insertion/removal
• Backward compatibility with Gen 1 LTSSM
• Full support for LPM commands, LFPS and LPBM

Note: Analog re-drivers and “bit level” re-timers are out of scope.

High-level schedule: Spec available by the end of the year
Summary of PHY Changes for Gen 2 Operation

- Reference transmitter with 3 taps
- Reference receiver with 7 CTLE boost settings and a 1-tap DFE
- JTOL corner frequency raised to 7.5MHz
- New 128b/132b encoding
- New ordered sets that are mostly scrambled
- New LFPS signaling requirements
- Addition of re-timing repeater requirements
Seminar Agenda

8:00  Registration check-in
9:00  Introduction to 10Gbps SuperSpeed USB
9:20  Architectural Overview
10:00 Break
10:30 Cables and Connectors
11:00 Physical Layer
12:00 Lunch
1:00  Link Layer
2:00  Protocol Layer
2:30  Break
3:00  Hub
4:00  Compliance
4:15  Q&A Session
4:30  Close
Link Layer

- Goals
- SS Performance Recap
- Link Layer Challenge
- Architectural Framework
  - 128b/132b
  - Packet Framing
  - Traffic Class
- LTSSM update
- Summary

Huimin Chen
Intel

Peter Teng
Renesas
Link Layer Goals

• Preserve SS link layer architecture with minimum changes – TTM
  – Same link flow control and data integrity → extend only
  – Similar strong quad packet framing → robustness
  – Same LTSSM structure → modularized add-ons

• Equal or better error performance compared to SS
  – Equal → same probability of error Recovery
  – Better → Single-bit error not going to Recovery

• Forward looking with maximum flexibility
  – LFPS based start-up speed negotiation to highest common port capability

Go faster with better energy efficiency, better error performance, and better extensibility but with minimum architectural changes
SS Error Performance: Recap

• Figure of merit of operational robustness:
  – Bit error rate (physical layer)
  – Retry: near-zero performance impact (link layer)
  – Recovery: significant (from few μs to few tens of μs) (PHY/Link layer)

• Probability of entry to Recovery due to bit error: \(5.7 \times 10^{-15}\)
  – The construction of SKP OS not single bit error tolerant
  – SLC not tolerant of single bit error

• Original SS goal: single bit error not going to Recovery
  – Probability of 2-bit error going to Recovery < \(8.0 \times 10^{-22}\)
  – 1e+7 more robust \(\rightarrow\) more tolerant of bit errors

Opportunity exists for SSP performance enhancement
10Gbps Challenge at the Link Layer

• Feasibility study at PHY layer suggests
  – 10Gbps preferred: better coexistence with 5Gbps $\rightarrow$ no architectural impact to the link layer
  – Random BER at 1e-12 based on AWGN still assumed $\rightarrow$ no additional error detection/correction mechanism needed
  – 8b/10b replaced with 128b/130b: DC balance and transition density manageable with data scrambling $\rightarrow$ significant impact to the link layer!

• 8b/10b:
  – Foundation of SS packet framing
  – The unique K-code mutually exclusive with D-code offers an explicit identification for packet framing

• 20% BW overhead is becoming too high if just for packet framing

Can the link layer architecture be preserved with energy efficient 128b/130b?
Introduction to 128b/132b Line Code

• A 132-bit block with 16 bytes non-encoded payload and 4-bit of block header
• Two blocks are defined
  – Control block (1100): TS1, TS2, TSEQ, SYNC, SKP, SDS
  – Data block (0011): packets, link commands, idle symbols (all scrambled inclusive of framing ordered set)
• 4-bit block header for block alignment and with good error tolerance
  – Single-bit error: self correctable
  – Two-bit error: detectable

Note: if 128b/130b is to be used, the probability of error Recovery due to single bit error is ~1.4e-14 → 2.6x worse than SS!

128b/132b code divides a bit stream into blocks with each block containing a block header
SSP Packet Construction

• Challenge to packet construction with 128b/132b code
  – No distinctive symbols for framing ordered set → can only be shared with data
  – Possible packet data (e.g. DPP) matching framing ordered set → if declared, can be catastrophic

• What we want:
  – Quad packet framing based on shared data symbols and still tolerant of single symbol error
  – Stop the framing ordered set detection within packet data

• Solution: protect packet boundary under single bit error
  – Boundary awareness to allow Rx to decide when to do packet framing detection
  – Boundary protected under single-bit error condition → optimize for robustness
  – Boundary unprotected under double or multi-bit error condition → symbol stream ambiguous → recover for simplicity

  Note: For the same block size, double bit error rate is 10~11-orders of magnitude lower than single bit error rate

It is feasible to preserve SS packet structure with 128b/132b code
SSP Packet Structure

• SS packet boundary study
  – All framing ordered sets tolerant of single symbol error → keep
  – Header packet/link command with fixed length: boundary protected under single bit error → keep
  – DPP has variable length
    • Boundary protected if (1). DPH not corrupted, and (2). DPP not truncated → keep
    • Boundary unknown if (1). DPH data corrupted under single bit error, or (2). DPP truncated → change needed

• SSP packet construction:
  – Framing OS: direct mapping from 10b domain to 8b domain
  – DP enhancement:
    • Non-deferred DPH to have its own framing OS (not to share with HP framing OS)
    • DPH length field to be tolerant of single bit error (new)
    • Outgoing DPP not to be truncated (new)

*Note: Deferred DPH to use HP format w/o length field replica*

SSP packet construction is consistent with SuperSpeed
Type 1/Type 2 Traffic Classes

• Motivation: packet prioritization for multi-stream traffic management

• Definition
  – Type 1 traffic class (Type 1 packet): TP, LMP, ITP, periodic DP, deferred DPH
  – Type 2 traffic class (Type 2 packet): asynchronous DP
  – Type 1 traffic class has higher priority over Type 2 traffic class

• Rx Buffer Credit to replace Rx Header Buffer Credit
  – Rx Buffer Credit: the amount of Rx buffer to store a DP of max DPP size
  – Rx Buffer Credit consumption tied to DP
  – Rx Buffer Credit return upon the availability of a Rx Buffer Credit

• Flow control
  – Type 1 traffic class is managed by LCRD1_x (x=A,B,C,D)/Type 1 CREDIT_HP_TIMER
  – Type 2 traffic class is managed by LCRD2_x (x=A,B,C,D)/Type 2 CREDIT_HP_TIMER
  – Extension of Header Sequence Number range from 0~7 to 0~15 (ECR)
  – Flow control of the two traffic classes are independent
  – The mechanism of flow control is the same as SS

All changes are incremental
Link Error Statistics

• Motivations
  – To monitor the error condition of link operation and re-configure the link for quality of service
  – To provide a mechanism for debugging

• Definition
  – Link error count: number of error events that result in link entering Recovery
  – Optional soft error count: number of single bit error detected at PHY, Link, and optionally Protocol (CRC32 error)

• Operation
  – SW accessible
  – Required by both DSP and USP
  – Reset upon power on, entry to U0 from Polling, Hot Reset, or directed
  – Saturate at 65,535

Comprehensive link error statistics offers an opportunity for data rate re-configuration to achieve optimized link operation
Link Command/SKP OS Error Tolerance

• Link command
  – Same structure but with different declaration of valid link command
    • SuperSpeed link command word replica not tolerant of single bit error
    • SuperSpeedPlus link command word replica tolerant of single bit error

<table>
<thead>
<tr>
<th>Valid link command</th>
<th>Link Framing OS</th>
<th>LCW1</th>
<th>LCW2</th>
<th>LCW1=LCW2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SuperSpeed</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Yes</td>
</tr>
<tr>
<td>SuperSpeedPlus</td>
<td>Valid</td>
<td>Valid</td>
<td>Invalid</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>Invalid</td>
<td>Valid</td>
<td>Invalid</td>
<td>No</td>
</tr>
</tbody>
</table>

• SKP OS transmitted as a control block tolerant of single bit error

The improved error tolerance of link command and SKP OS have made it possible for robust SSP operation with single bit error not going to Recovery
Start-up Speed Negotiation Protocol

• **Motivations**
  – Performance: minimize initialization latency by starting at highest possible rate
  – Compatibility: preserve maximum interoperability with SS host/device
  – Flexibility: reserve options for future generations to be more configurable without need to be tied to legacy

• **Mechanism: LFPS based port capability announcement and negotiation**
  – SCD1.LFPS/SCD2.LFPS (SS Capability Declaration) for SS compatibility and SSP identification
  – LBPM (LFPS based PWM Message) for port capability negotiation
New Sub-states in Polling

Polling.LFPSPlus – extended Polling.LFPS for SCD* handshake
• SCD1/SCD2 patterns chosen for more distinction

Polling.PortMatch
• Port capability announcement, and negotiation
• Exit on common LBPM PHY Capability handshake

Polling.PortConfig
• PHY re-configuration
• Exit on LBPM PHY Ready handshake

<table>
<thead>
<tr>
<th>b1~b0: LBPM Type</th>
<th>b3~2: LBPM Subtype</th>
<th>00: PHY Capability</th>
<th>00: 5Gbps</th>
<th>01: 10Gbps</th>
<th>b7~b4: Reserved (0000)</th>
<th>01: PHY Ready</th>
<th>Reserved (01)</th>
</tr>
</thead>
</table>

Minimum LTSSM change

Add-on sub-states to Polling

Training failure leads to port negotiation to the next common capability
Polling substrates: examples

**SSP to SSP: from Polling.LFPS to Polling.RxEQ**

- LP1 (Gen 2): ...
  - SCD1
  - Polling.LFPS
  - SCD1
  - Polling.LFPS
  - SCD1
  - Polling.LFPSPlus
  - SCD2
  - EI
  - Polling.PortMatch
  - TSEQ

- LP2 (Gen 2): Rx.Detect
  - SCD1
  - Polling.LFPS
  - SCD1
  - Polling.LFPS
  - SCD1
  - Polling.LFPSPlus
  - SCD2
  - EI
  - Polling.PortMatch
  - TSEQ

**SSP to SS: start at SSP, detect SS, switch, and exit to SS operation**

- LP1 (Gen 2): ...
  - SCD1
  - Polling.LFPS
  - Detect SS
  - Switch to SS
  - TSEQ

- LP2 (Gen 1): Rx.Detect
  - Polling.LFPS
  - Constant tRepeat
  - 60us LFPS EI detection, or Polling.LFPS handshake
  - TSEQ
Summary

<table>
<thead>
<tr>
<th></th>
<th>SS</th>
<th>SSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line code</td>
<td>8b/10b</td>
<td>128b/132b</td>
</tr>
<tr>
<td>BW overhead</td>
<td>20%</td>
<td>3%</td>
</tr>
<tr>
<td>Data rate (Gbps)</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Random BER</td>
<td></td>
<td>1e-12</td>
</tr>
<tr>
<td>Probability of Recovery entry due to single-bit error</td>
<td>5.7e-15</td>
<td>0</td>
</tr>
<tr>
<td>Probability of Recovery entry due to single/multi-bit error</td>
<td>&gt; 5.7e-15</td>
<td>1.8e-22</td>
</tr>
</tbody>
</table>

- USB 3.0 SS is a proven example of a working link layer
- The SSP introduction of 128b/132b line code with 4-bit sync header
  - Complements SS USB’s strong packet framing to achieve single-bit error not going to Recovery
  - Preserves the link layer architecture with minimum change
- LFPS based start-up speed negotiation protocol minimizes the initialization latency while offering maximum flexibility for port configuration
Link Layer ECRs

- Header Sequence Number Extension for SSP

From Text:

A deferred SuperSpeedPlus data packet header shall always begin with HPSTART ordered set and it shall contain the length field replica.

To Text:

A deferred SuperSpeedPlus data packet header shall always begin with HPSTART ordered set and it shall **NOT** contain the length field replica. A deferred DPH, whether periodic or asynchronous, shall always be type 1 traffic class.

Editorial

Section 7.2.1.1.1
Protocol Layer

- Effects of mixed speed traffic through a hub
- Speed reporting
- Deprecated features

Bob Dunstan
Intel
Sue Vining
TI
Maximizing Bandwidth Utilization

Example of mixed speed hub connections

**When:** Data packet from Gen 1 Downstream-Facing Port (DFP) through Gen 2 Upstream-Facing Port (UFP) of hub

**Why:** To recover bandwidth on UFP as DFP fills

**How:** Host may issue concurrent IN requests, but not to same Gen 1 DFP

**What:** Hubs must arbitrate among data packets from multiple DFPs
Packet Arbitration

- Fair arbitration independent of hub depth requires weighting
  - Weight value is reported through lower 16 bits of area reserved for 20-bit Route String field
  - Route String/Weight field rules are defined by hub
- Arbitration can cause reordering among endpoints, but not for same endpoint
Honoring Periodic Contracts

**When:** Latency of completing async transactions through Gen 1 DFP of hub with Gen 2 UFP delays periodic transactions

**Why:** Meet periodic schedule

**How:** Hub prioritizes periodic data above async data from host

**What:** Transactions can get reordered, when async OUTs get delayed behind periodic OUTs. Also uses Transaction Type field in DPH.
Arbitration and Transfer Types

- Arbiter prioritizes periodic data to meet scheduling
  - Requires knowledge of transfer type
    - Transfer type must be validated for received packets
    - TT field added to TP and DPH packets at offset DW 1: bit 12

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>100b</td>
<td>Control Transfer Type</td>
</tr>
<tr>
<td>101b</td>
<td>Isochronous Transfer Type</td>
</tr>
<tr>
<td>110b</td>
<td>Bulk Transfer Type</td>
</tr>
<tr>
<td>111b</td>
<td>Interrupt Transfer Type</td>
</tr>
</tbody>
</table>

- Requires change to link level flow control and credits
  - Num HP Buffers field in Port Capability, Port Configuration and Port Configuration Response LMPs is unused and set to zero for SuperSpeedPlus
Changes to Timing Parameters

- Timing parameters changed and added
  - `tHostTransactionTimeout` 7.6ms min/25ms max
  - `tGen2MaxBurstInterval` 50ns
  - `tGen2MaxDeviceMultiPacketInterval` 50ns
  - `tGen2MaxHubMultiPacketInterval` 50ns
  - `tHostTPFTimeout` 7.6ms min/25ms max
  - `tDeviceTPFNotification` 400ns
  - `maxtITPRegenerationLimit` -0 μs min/-33μs max
  - `tLDMRequestTimeout` 125μs
  - `tLDMResponseDelay` 125μs
  - `tLDMResponseTime` 3μs
  - `tTPTransmissionDelay` 40ns
Speed Reporting for Gen 2 Operation

- Inform host HW of speed to do scheduling without new SW
  - TPF field at offset 1:31 in TP ACK for Status TP
  - Link Speed Device Notification packet

<table>
<thead>
<tr>
<th>Host</th>
<th>Device (peripheral or hub)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status TP for Set Address request</td>
<td></td>
</tr>
<tr>
<td>Wait for L.S.D.N.</td>
<td>TP ACK with TPF set</td>
</tr>
<tr>
<td>End wait for L.S.D.N.</td>
<td>Link Speed Device Notification packet</td>
</tr>
</tbody>
</table>
Speed Reporting for Gen 2 Operation

- Link Speed field in Port Capability, Port Configuration and Configuration Response LMPs is unused and set to zero for Gen2
  - LBPM addresses speed negotiation and reduces the time to establish the link speed
Depreciated Features

- Bus Interval Adjustment (BIA) Message Device Notification
  - Allowed only for Gen 1 operation
  - Disallowed for Gen 2 operation

- Precision Time Measurement (PTM) augments ITP functionality
  - Similar mechanism as defined in IEEE 1588-2008 and IEEE 802.1AS-2011
Framework changes

All devices need to return 0x0310 in the Specification Revision field of the Device Descriptor

Precision Time Measurement

• Protocol for determining propagation delays through the USB topology
  • Through hubs and over individual links
• Updated Get Status command to return
  • Link Delay Measurement (LDM) Enabled/Disabled Status
  • LDM Valid
  • 16 bit Link Delay Value if LDM is Enabled and Valid
• Use SetFeature and ClearFeature to Enable/Disable LDM
Framework changes

- PLATFORM (operating system/OEM/ODM)
  - Contains a 128-bit UUID value
  - Defined and published independently by the platform/operating system vendor
  - Used to identify a unique platform specific device capability
- SUPERSPEED_PLUS
  - Describes the speeds/lanes at which this device operates
- PRECISION_TIME_MEASUREMENT
  - The presence/absence of this descriptor is used to determine if the device supports PTM

Added support for larger ISO Endpoints

- Meaning of wBytesPerInterval in EP Companion Descriptor depends on the value of SSP ISO Companion (SSP-IC) bit
  - If SSP-IC is set to zero: Determines the bus time to reserve per SI
  - If SSP-IC is set to one: the dwBytesPerInterval in the SSP Isochronous Endpoint Descriptor determines the bus time to reserve per SI
Seminar Agenda

8:00  Registration check-in
9:00  Introduction to 10Gbps SuperSpeed USB
9:20  Architectural Overview
10:00 Break
10:30 Cables and Connectors
11:00 Physical Layer
12:00 Lunch
1:00  Link Layer
2:00  Protocol Layer
2:30  Break
3:00  Hub
4:00  Compliance
4:15  Q&A Session
4:30  Close
Hub

- USB 3.1 Hub Architecture
- Why change?
- Buffering & Arbitration
- Summary

Rahman Ismail
Intel

John Garney
MCCI
USB 3.1 Hub Architecture

SuperSpeedPlus, SuperSpeed and USB 2.0 device support

Upstream facing port connects at Gen 1 speed
- Hub operates as a SuperSpeed hub
- Downstream ports support SuperSpeed and USB 2.0

Upstream facing port connects at Gen 2 speed
- Hub operates as a SuperSpeedPlus hub
- Downstream ports support all speeds
SuperSpeed Hub Architecture

SuperSpeed Hub Repeater/Forwarder
- Responsible for the behavior of upstream/downstream ports
- Minimal buffering of each packet received from upstream/downstream links
- Transmitting packets on upstream/downstream links
- Routing packets

SuperSpeed Hub Controller
- Responsible for host-to-hub communication
SuperSpeedPlus Hub Architecture

SuperSpeedPlus Upstream Controller
- Responsible for the behavior of the upstream port
- Buffering packets being received from the upstream link
- Buffering and Arbitrating packets waiting to be transmitted on the upstream link
- Routing packets to the appropriate destination
SuperSpeedPlus Hub Architecture

SuperSpeedPlus Downstream Controller
- Responsible for the behavior of the downstream port
- Buffering packets being received from the downstream link
- Buffering and Arbitrating packets waiting to be transmitted on the downstream link
- Routing packets to the upstream port controller

SuperSpeedPlus Hub Controller
- Responsible for host-to-hub communication
Motivation for Hub Change

Maximize upstream bandwidth usage

Provide primitives for smart host scheduling
- Comprehend transfer types (Async vs. Periodic)
- Propagation of DPs received from downstream ports
  - Higher priority to Periodic traffic
  - Round robin for Periodic DPs
  - Weighted round robin for Async DPs
- Propagation of TPs received from downstream ports
  - First come first served
  - Sent before any DPs are transmitted

Power Efficient Solution
- Utilize U1 and U2 as much as possible
Performance Penalty

One-IN-at-a-time rule

- Performance will be compromised

Results in a 33% loss of bandwidth

Pros:
- Uses Existing Protocol
- Minimal changes to the host scheduler
Where Do We Want to Get?

Maximize upstream bandwidth usage
- Multiple outstanding INs

Preserve Periodic traffic contract
- Need to determine packet priority
- Modify Packet Arbitration Weight when propagating upstream
Packet Priority

A and D are Periodic

- A: 39 Packets per μFrame (operating at Gen1)
- D: 78 Packets per μFrame (operating at Gen2)

B and C are Asynchronous devices
Increased Buffer Requirements

**Upstream Flow**
- 16KB DPP Async per DFP receiver
- 16KB DPP Periodic per DFP receiver
- 16 DPH Async & 16 DPH Periodic per DFP receiver

**Downstream Flow**
- 18KB Async per Hub
- 18KB Periodic per Hub
- 18 DPH Async & 18 DPH Periodic per Hub
Hub Packet Forwarding

Problem
Scenario:
- 3 hubs daisy chained together
- Each hub has 2 Async SuperSpeed devices connected to a DFP
- All Async devices will use as much bandwidth as available

Problem:
- Per-port weighted round robin forwarding algorithms will give more bandwidth to devices located further upstream

Solution:
- Use an algorithm which accounts for the number of devices downstream
  - Only count currently transmitting devices
Per-Port Weighted Round Robin Algorithm

- Weighted round robin, where each port is given a weight
- Ports take turn forwarding, where faster ports get proportionally more turns
- Weight of the port dependent on the speed of the device
  - 5G = 4
  - 10G = 8
Per Port WRR Algorithm: Results

Highest devices each received 33% of available bandwidth
Lowest devices each received 5.5% of available bandwidth
Bandwidth given to devices depends upon location on the bus

2 Packets from devices directly connected to the hub are sent for every packet forwarded from a lower hub
Async Weighted Sum Algorithm

- Weighted round robin, where each packet gets a weight
- Ports take turn forwarding, where ports with heavier packets get proportionally more turns
- Initial Weight of the packet dependent on the speed of the link
  - 5G = 4
  - 10G = 8
- Weight of forwarded packet from hub is sum of all active downstream devices weight
Async Weighted Sum-Based Algorithm: Results

All devices forward approx. the same number of packets per service interval.

Bandwidth given to devices independent of location on the bus
TP Labeling/Credit

Separated Async/Periodic link level flow control

- Requires TP Async/Periodic Labels
  - Transfer type labels: control, isoch, int, bulk
- Require Async/Periodic Credit
  - LCRD1_X for Periodic DP/TP/LMP
  - LCRD2_X for Async DP
- 4 credits for Async, 4 credits for Periodic

Track OUT/IN to SuperSpeed bus instances

- Add transfer type label for response DPHs

December 10, 2013
SuperSpeedPlus Hub Arbitration

TPs prioritized over DPs
• Both Directions: Upstream & Downstream

Periodic DPs prioritized over Async DPs
• Both Directions: Upstream & Downstream

Async DPs Weighted Fair Share Round Robin
• Upstream DPs carry summed weight
  – 16 bit weight field
  – Using 16 bits in the reserved RouteString space

Arbitration occurs close to end of current Packet transmission
Summary

Support all types of devices
- SuperSpeedPlus, SuperSpeed and USB 2.0 devices

Maximizes upstream bandwidth usage

Uses a Store and Forward model

Supports smart host scheduling

Provides support for fair service of Async flows
Compliance

• Areas of change
  • Cable and Connector
  • Electrical/PHY
  • Link Layer
  • Interoperability
  • Framework
  • Hubs

• Interoperability

• Timeline

Rahman Ismail
Intel
Compliance – Link Layer

Link Layer LTSSM is relatively unchanged between USB 3.0 and USB 3.1
• Major changes underlie the link layer
  – Test implementation must be entirely reworked from a Link Verification System standpoint
• Link Training differences make up the bulk of test step changes

Chapter 6 test changes will include:
• TD 6.2 Skip OS Test
  – USB 3.1 SKP Ordered Sets are very different from its predecessor
  – Verify successfully receiving anywhere from 0 to 36 SKPs in a SKP OS
• TD 6.6 SCD1 / SCD2 Duration Test
  – Verify training against a range of SCD1/SCD2 tburst and trepeat parameters
• TD 6.7 LBPM Parameters Test
  – Verify LBPM with a range of tPWM and tLFPS-0/tLFPS-1 parameters
Chapter 7 test changes will include:

- **TD 7.3. Link Commands CRC-5 Robustness Test and TD 7.4 Invalid Link Commands Test**
  - USB 3.1 Link Commands are valid if at least one of the LCWs is valid with a correct CRC-5

- **TD 7.15 Wrong LCRD_X Sequence Test**
  - USB 3.1 uses LCRD1_X and LCRD2_X. Test cases will be added accordingly

- **TD 7.1 and TD 7.26 checks LTSSM state changes from Rx.Detect to U0 or from Recovery to U0**
  - USB 3.1 uses a new SDS Ordered Set for Polling.Idle, Recovery.Idle
  - Will reflect USB 3.1 definitions for TSEQ, TS1, TS2 Ordered Sets and new SYNC Ordered Set
  - Add Gen 1 and Gen 2 training together checks – fallback from Gen 2 to Gen 1 in Polling.LFPS (may extrapolate to new TD)

- **TD 7.39 PortMatch Negotiation Test**
  - Check that a port can renegotiate speeds during Polling.Active and Polling.Configuration
Compliance - Framework

Confirm transitions between SS and SSP
GetStatus, SetFeature, ClearFeature

- LDM_ENABLE feature selector
- PTM_STATUS new status type

BCD version number change: 0x0310
Compliance – Framework

New device capability types

- PLATFORM
- SUPERSPEED_PLUS
- PRECISION_TIME_MEASUREMENT

Endpoint Companion Descriptor

- wBytesPerInterval changes

SSP Isochronous Endpoint Descriptor
Compliance – Enhanced SuperSpeed Hubs

- New DFP States
- SSP Store and Forward Behavior
- Arbitration of Packets
- Extended Port Status
- Transitions between SS and SSP
- Descriptor changes
## Compliance – Sample Assertions

### Subsection reference: 10.1 Hub Feature Summary

| 10.1#1 | All exposed downstream ports on an Enhanced SuperSpeed hub shall support both Gen X and USB 2.0 connections. | 3.0 Hub tests and 2.0 Hub tests. |
| 10.1#2 | Hub detects device connect and disconnect | Multiple tests |
| 10.1#3 | When an Enhanced SuperSpeed hub connects on its upstream facing port at Gen 1, its downstream ports shall connect no higher than Gen 1. | TD 10.23 |
| 10.1#4 | Hubs shall only provide power to DS ports if the US port is connected, or the hub supports Battery Charging. | Hub LVS |
Compliance – Sample TD

TD 10.23 Hub Downstream Port Operating at Gen1
This test verifies that the downstream port of a Gen2 capable hub will only operate a speed less than or equal to the upstream hub port.

Assertions Covered
10.1#3, 10.1.1#4

Starting Configuration
Port Under Test: SuperSpeedPlus Capable Device
Auxiliary Ports: No Device Attached

Test Steps
1. Attach hub to a host port that only supports Gen1 speeds.
2. Enumerate and configure the Hub.
3. Test fails if hub does not enumerate at SS Gen1 speed. (10.1.1#4)
4. Prompt user to attach an Enhanced SuperSpeed device with Gen2 capability to a hub DS port.
5. Enumerate the attached device.
6. Test fails if DS device enumerated at Gen2 speed. (10.1 #3)
7. Test fails if DS device enumerated at FS or HS. (10.1.1#4)
Compliance – Interoperability
Compliance - Interoperability
Compliance - Interoperability
## USB 3.1 Compliance Timeline

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<tbody>
<tr>
<td>0.5</td>
<td>Test Assertions</td>
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<tr>
<td>0.7</td>
<td>Test Assertions + Test Descriptions</td>
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<tr>
<td>0.9</td>
<td>Tests coded and Test Specification updated</td>
</tr>
<tr>
<td>0.95</td>
<td>Beta tool release</td>
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<tr>
<td>1.0</td>
<td>Final tool release</td>
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### Milestones:
- **Q1 2013**: Test Assertions
- **Q1 2014**: Test Descriptions
- **Q4 2014**: Product Integration Lab (PIL) Testing
- **Q1 2015**: Test Tool Development
- **Q2 2015**: Test Tool Refinement
- **1.0 Compliance Spec Release**: First USB-IF workshop
- **ITL rollout**: ITL rollout
Q&A Session